22FDX: An Optimal Technology for Automotive and mmWave Designs

Venkat Ramasubramanian
Director, Customer Design Enablement

GLOBALFOUNDRIES®

Agenda

1. Introduction to GLOBALFOUNDRIES
2. FD-SOI transistor architecture
3. FinFET-like performance, Body-Biasing, ULP, ULL
4. 22FDX: 5G mmWave & Automotive readiness
5. Customer Design Enablement
6. Summary

Agenda

1. Introduction to GLOBALFOUNDRIES
2.
3.
4.
5.
6.

Semiconductors enable a connected future across markets & applications

Video
Images
Audio
Sensors

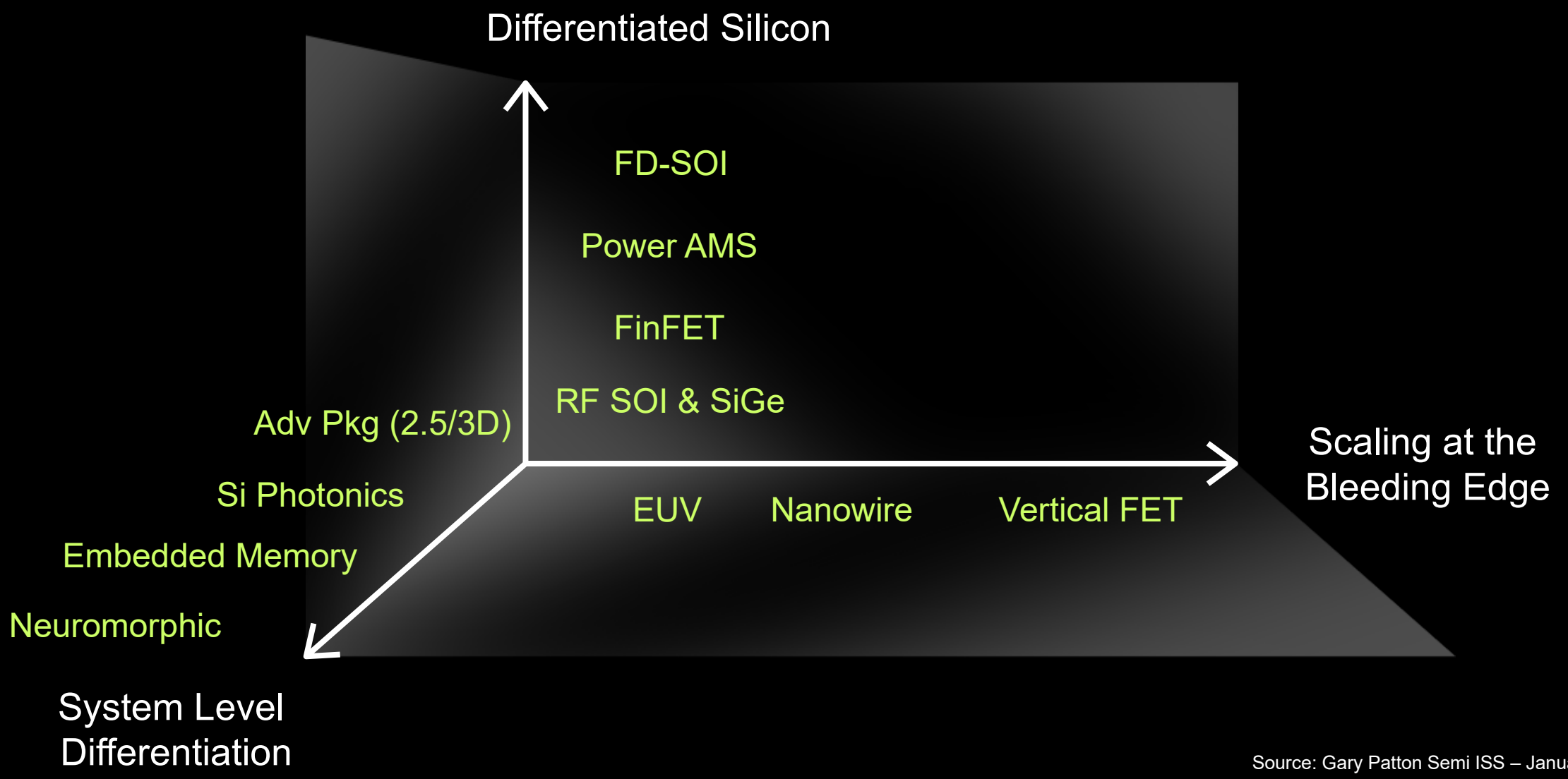
5G Wireless
Wi-Fi
Wired/ Optical
Satellite

Data Processing
Analytics
Prediction
Machine Learning

Replication
Storage
Access
Distribution

Next-Gen Mobile & IoT
ADAS &AR / VR Autonomous Vehicles
Base Stations
Microwave Backhaul
Edge Computing
Optical
5G / mmWave
Data Centers
AI / Machine Learning

New vectors of semiconductor innovation



Source: Gary Patton Semi ISS – January 2017

Paradigm Shift: Innovation shifting to differentiated features

AMS
- HV CMOS
- eNVM
- BCD/BCDLite®

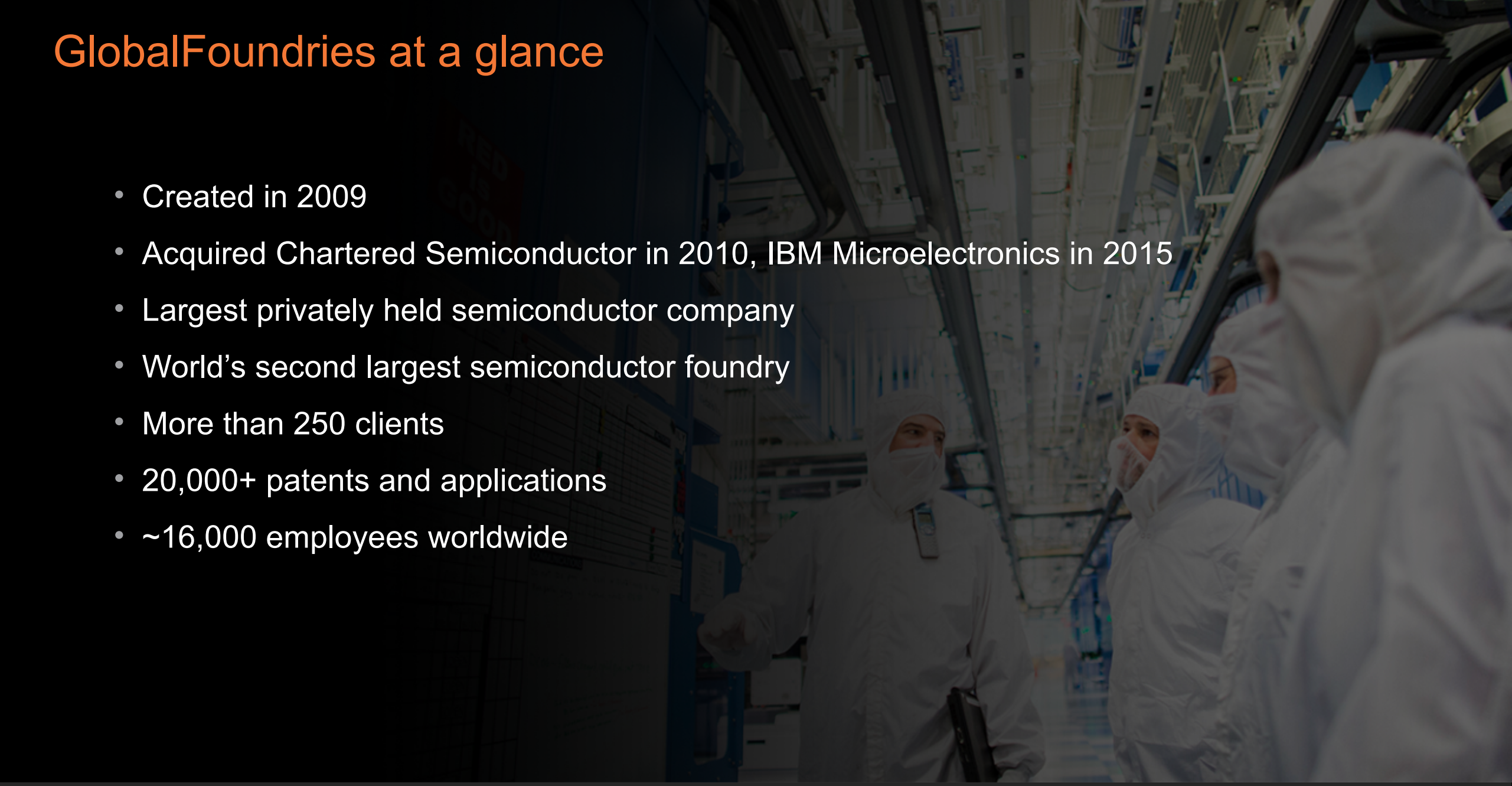
FDX™
- DigiRF & Analog
- mmWave
- eMRAM
- ULP ULL
- Back biasing

RF
- RF CMOS
- RF SOI
- mmWave
- SiGe PA
- SiGe HP

FinFET
- DigiRF & Analog
- Performance boost
- eNVM
- Ultra-high density
- Advanced packaging
- Advanced MIM

Emerging offerings
- SiPh

GlobalFoundries at a glance



- Created in 2009
- Acquired Chartered Semiconductor in 2010, IBM Microelectronics in 2015
- Largest privately held semiconductor company
- World’s second largest semiconductor foundry
- More than 250 clients
- 20,000+ patents and applications
- ~16,000 employees worldwide

Extensive suite of offerings and services

CMOS

Broad technology portfolio across leading-edge and mainstream nodes

RF

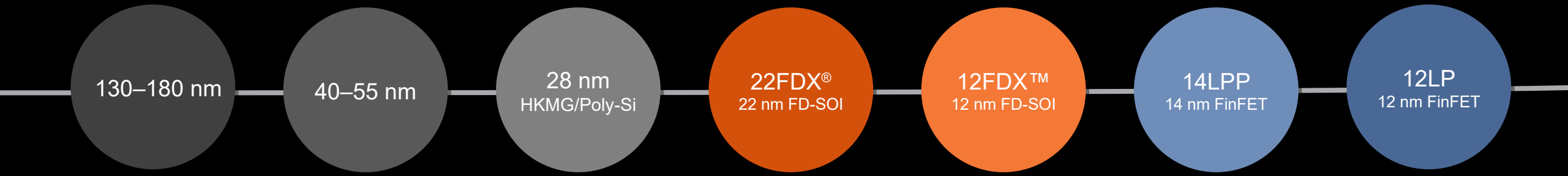
Comprehensive enablement and extensive, optimized RF portfolio including RF SOI and SiGe

Aerospace & Defense

Leverages offerings across the GLOBALFOUNDRIES portfolio to provide solutions for Trusted and Aerospace and Defense applications for both government and commercial markets

CMOS

Broad and differentiated product offerings



Mainstream

- 180 nm to 28 nm
- 200 mm, 300 mm wafers
- 28 nm HKMG/Poly-Si
  - Industry leader, over 1 million wafers shipped
- Mixed-technology offerings based on proven processes
- Analog/mixed-signal, RF/mmWave, high voltage (power management)
- RF CMOS, embedded memory, display drivers, MEMS

Performance

- FDX™ technology
  - Industry's first FD-SOI roadmap
  - Ideal for IoT, mainstream mobile, RF and power-efficient SoCs
- FinFET technology
  - Industry roadmap for highest performance and density
  - Ideal for high-end mobile, servers, graphics and networking
- Driving rapid migration to RF and embedded memory on leading-edge platforms

THINK RF? THINK GF! A Rich Platform for 5G Innovation

Sub 6 GHz
5G/4G

mmWave
28GHz+ 5G

5G

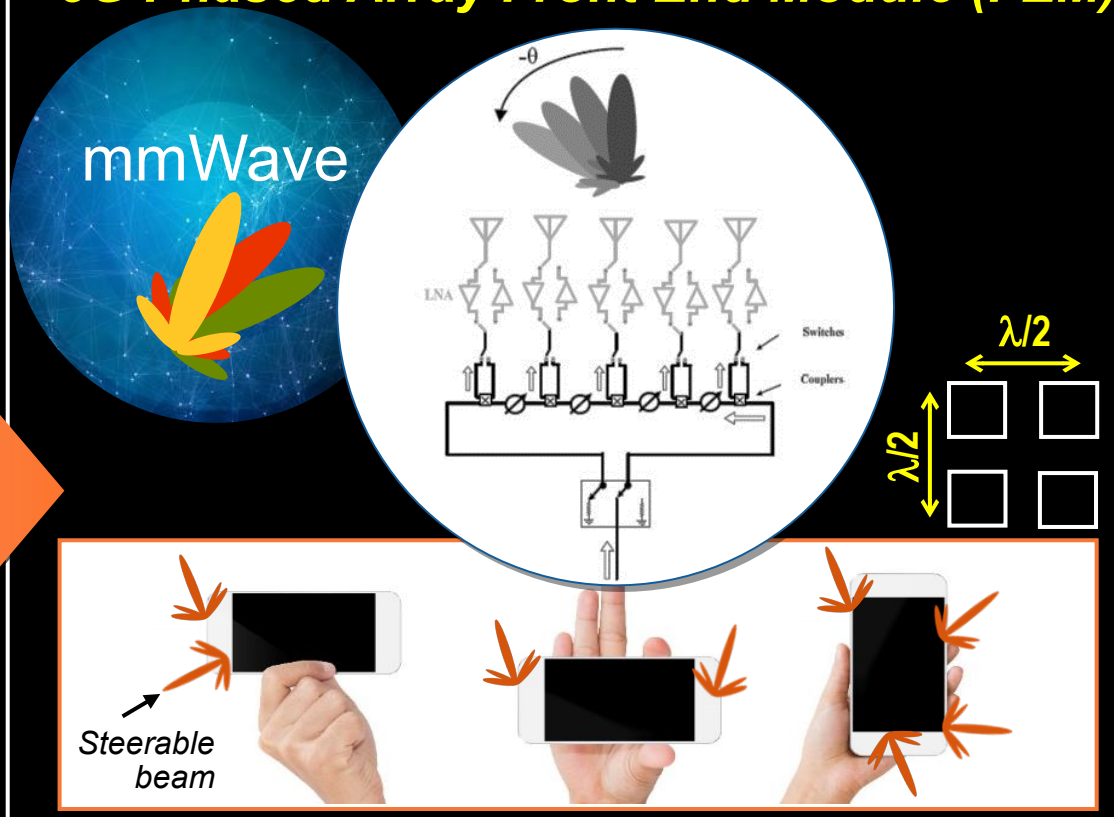
Mobile comms
Base stations

Phased arrays
Beamforming

7SW RF SOI
8SW RF SOI
SiGe HP

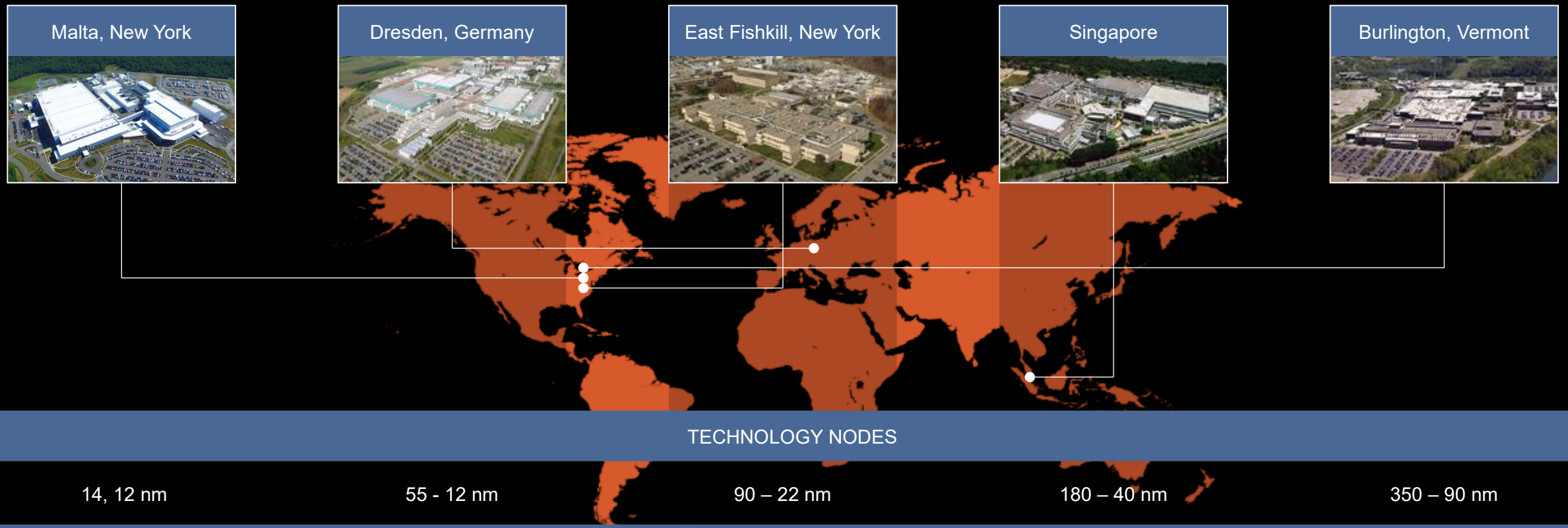
45RFSOI PD-SOI
22FDX® FD-SOI
SiGe HP

5G Phased Array Front End Module (FEM)



Highly focused, directional antenna beam
Secure & immune to interference
High data rates and user density/capacity

Worldwide manufacturing



TECHNOLOGY NODES				
14, 12 nm	55 - 12 nm	90 – 22 nm	180 – 40 nm	350 – 90 nm
WAFER SIZE				
300 mm	300 mm	300 mm	300/200 mm	200 mm

Agenda

1

2 FD-SOI transistor architecture

3

4

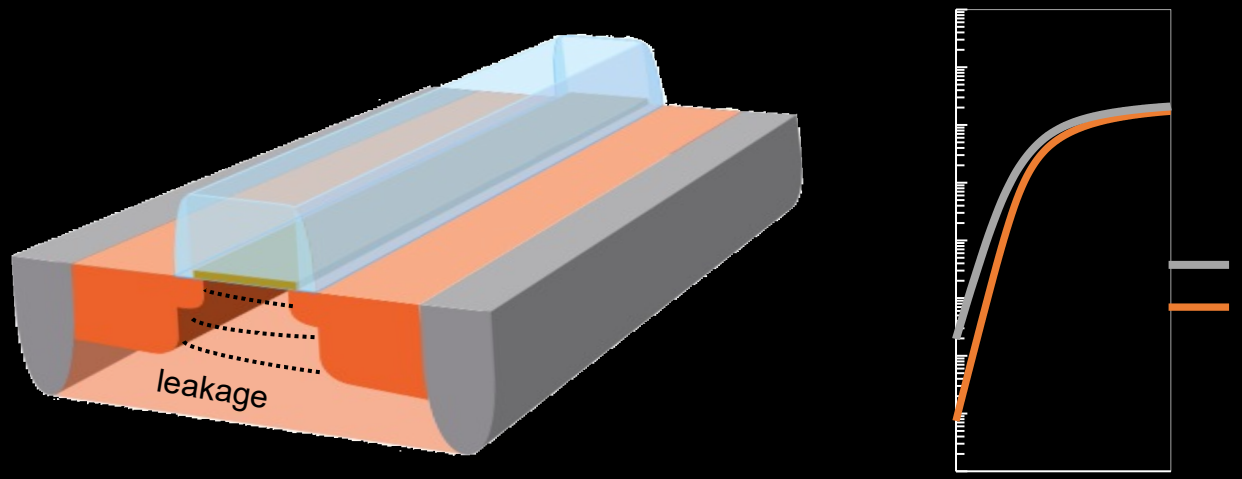
5

6

FD-SOI Continues Planar FET Scaling Beyond Bulk

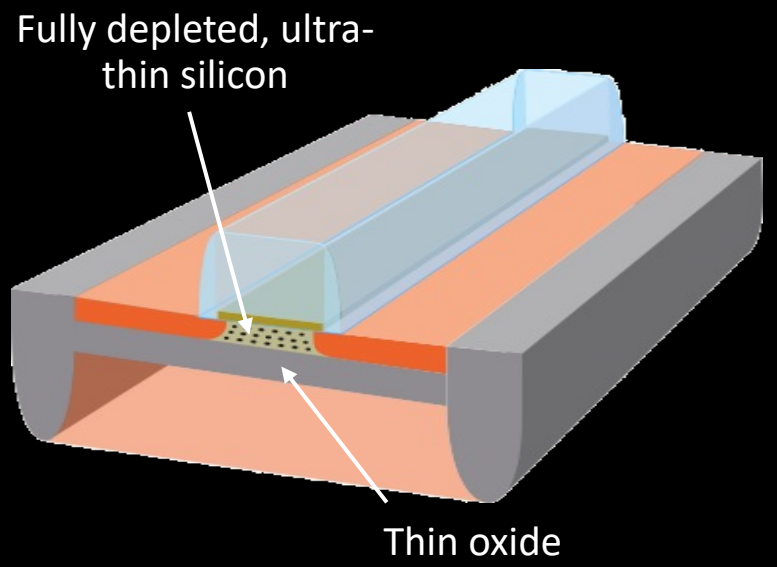
Enables truly sub-28nm gate length – with excellent short-channel effects control

Bulk CMOS



- Leakage path deep in bulk is under weak gate control
- Significantly degraded I_{ON}/I_{OFF} at gate length <28mm

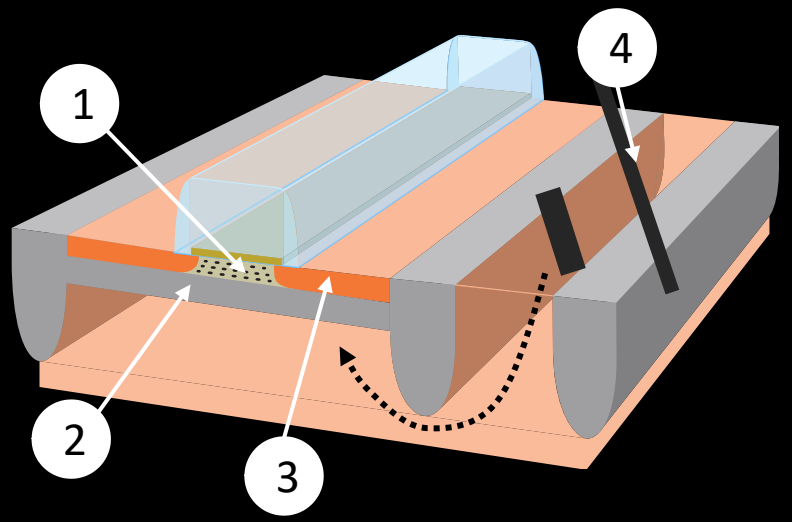
FD-SOI

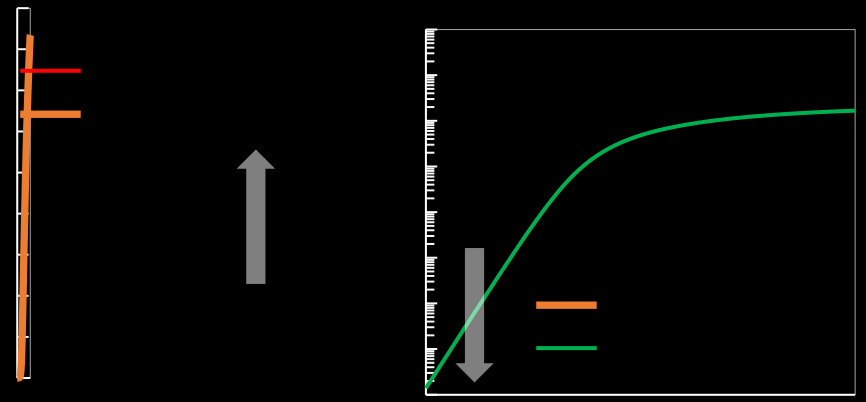


- Ultra-thin channel remains fully depleted & under full gate control
- Restores I_{ON}/I_{OFF} at gate length <28mm

Key Architectural Elements

Enabling superior digital, analog, and mmWave performance





	FD-SOI architectural element	*Replaces technology knobs in Bulk*	*Benefit*
1	Ultra-thin silicon	• Heavy channel doping; • Halo doping	• Reduced Random Dopant Fluctuation (RDF) effect • Better SCE control • Higher mobility
2	Thin buried oxide (BOX)	Heavy channel doping to set Vt	• Use of well to set Vt • Effective body bias • ~Little impact on thermal conductance
3	Ultra-shallow junction on BOX	Halo doping	• Reduced DIBL • Removal of bottom junction cap
4	Well (i.e. body), electrically isolated from channel	n/a	• Effective body bias • Extra design freedom

Agenda

1

2

3 FinFET-like performance, Body-Biasing, ULP, ULL

4

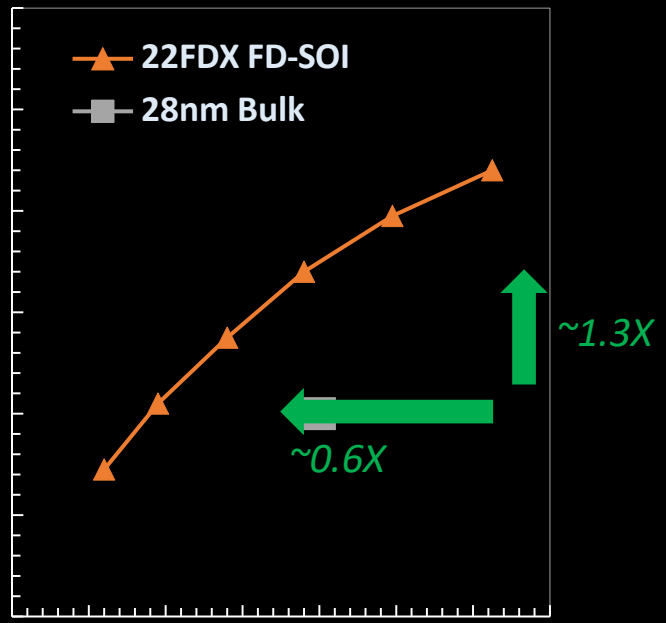
5

6

Full-node PPA Benefits over 28nm Bulk

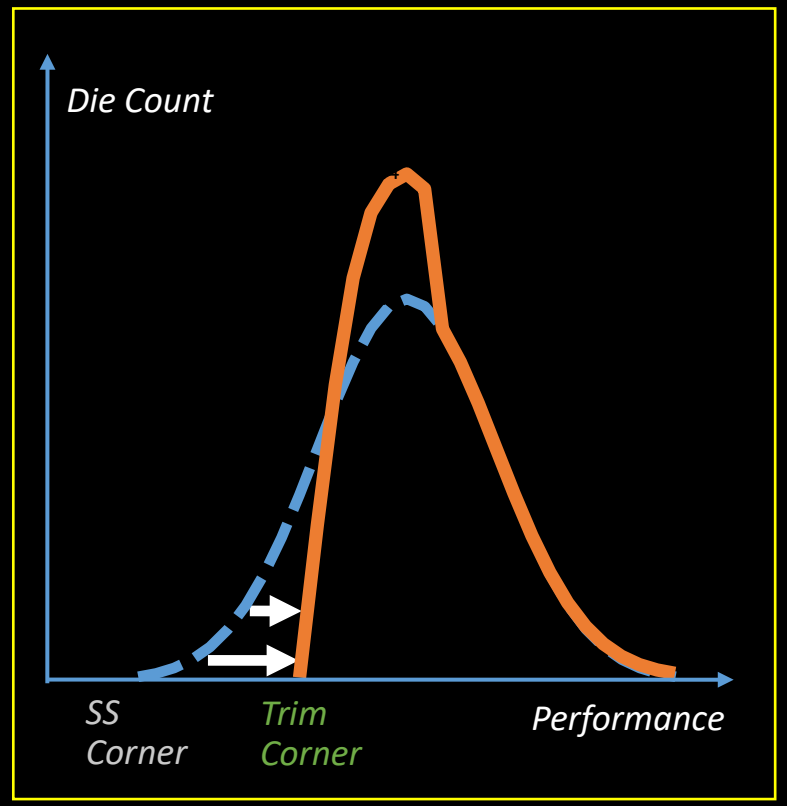
Enabled by sub-28nm gate length and superior subthreshold slope

	28nm HKMG	22FDX® FD-SOI
Vnom [V]	1.0	**0.8**
Contacted Poly Pitch	1.0	**<0.9**
M1 Pitch	1.0	**<0.9**
Perf @ Iso-Pwr TT, 25°C	1.0	**1.3**
Pwr @ Iso-Perf TT, 25°C	1.0	**0.6**

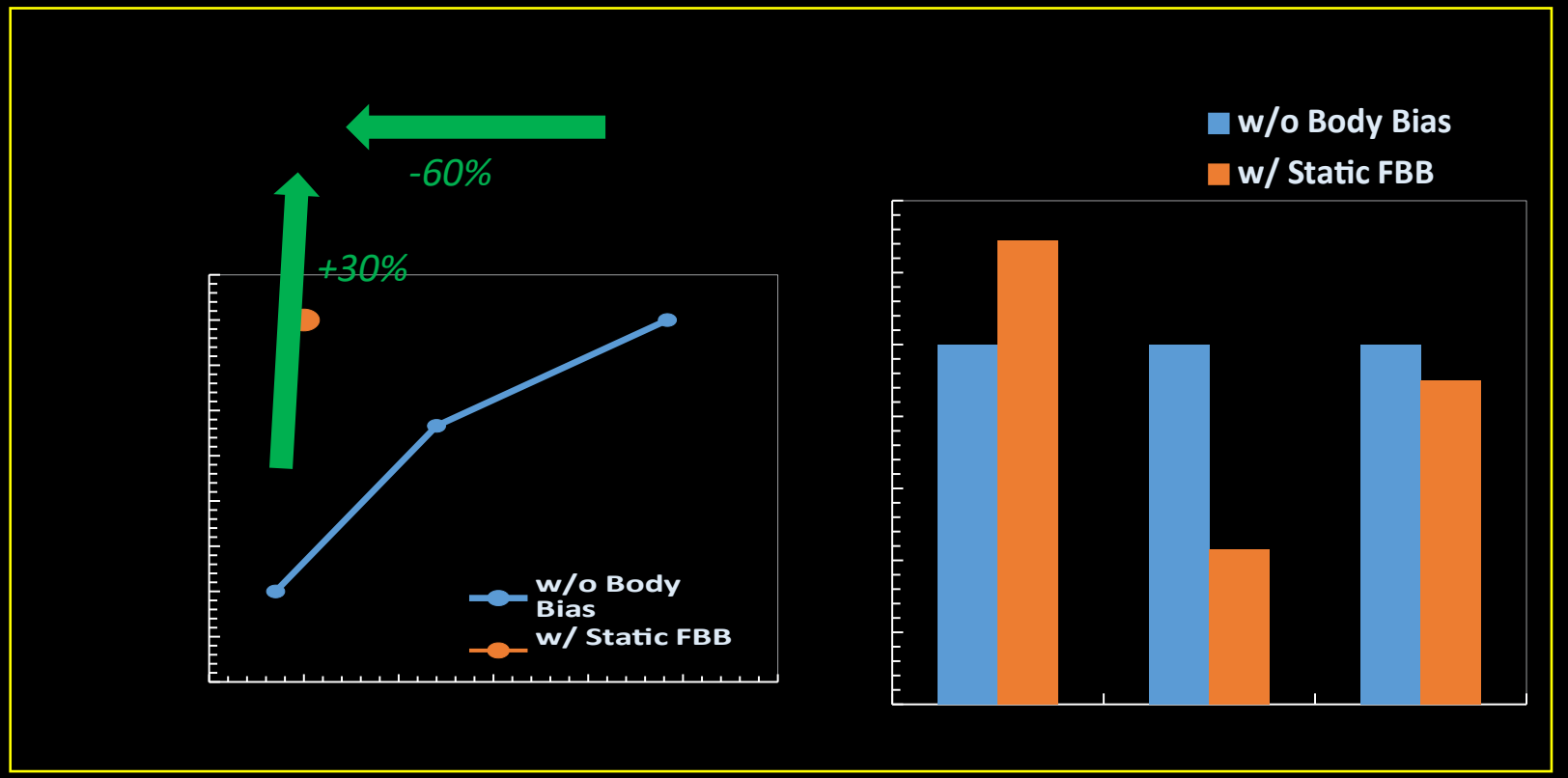


Static FBB Elevates Performance/Power Efficiency to FinFET Level

Up to *additional* 30% more performance, 60% lower power, *and* 10% smaller area



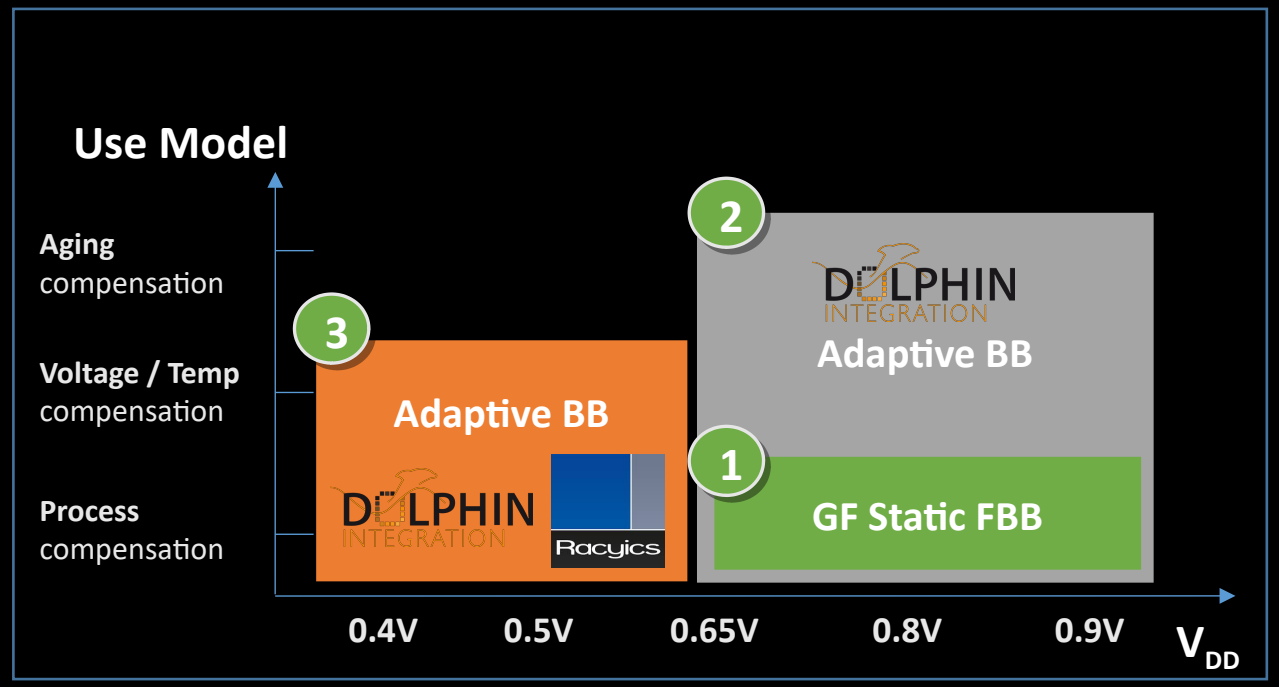
Static Forward Body Bias (FBB) Allows Timing Closure at Faster Corners



Example of Static FBB Implementation on Arm® Cortex®-A53 to Improve PPA

22FDX® Body Bias Solutions & Use Models

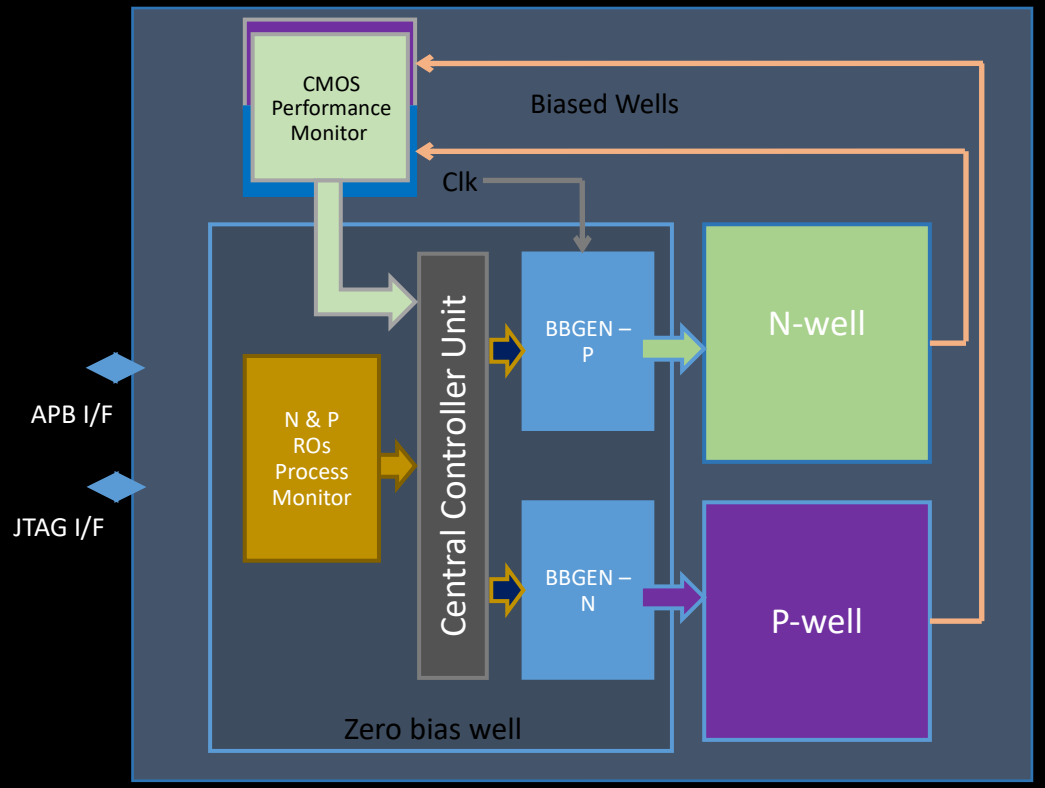
Static FBB in production; Platform Adaptive BB Solution ready NOW!



1. Static FBB works around nominal VDD & provides compelling PPA benefits
   - Applications: Smart audio, eMPU, MCU, A&D, 5G Infrastructure
   - 15-30% improvement Fmax @ same power
2. ABB @ nominal VDD offers meaningful benefit from aging compensation
   - Applications: Smart audio, eMPU, MCU, A&D, 5G Infrastructure
   - ~9% improvement in Fmax
3. ABB uniquely enables ultra-low-voltage through voltage, temperature, and process compensation
   - Applications: IoT connectivity, edge AI/ML, vision, ISP
   - Up to 7X energy efficiency gain

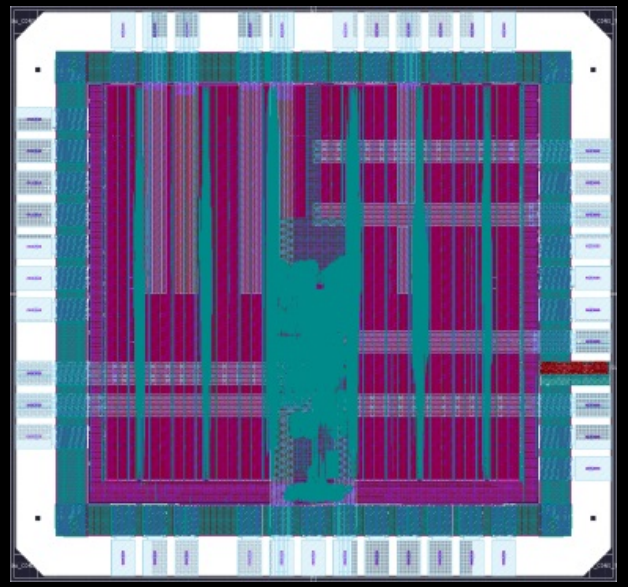
0.4V Ultra-low Power – Overcoming P/V/T Fluctuations

Enabled by Adaptive Body Bias (ABB)



Closed-loop Control to Provide Adaptive Body Bias

Arm® Cortex®-M4
Implemented by Racyics



1.5mm x 1.5mm

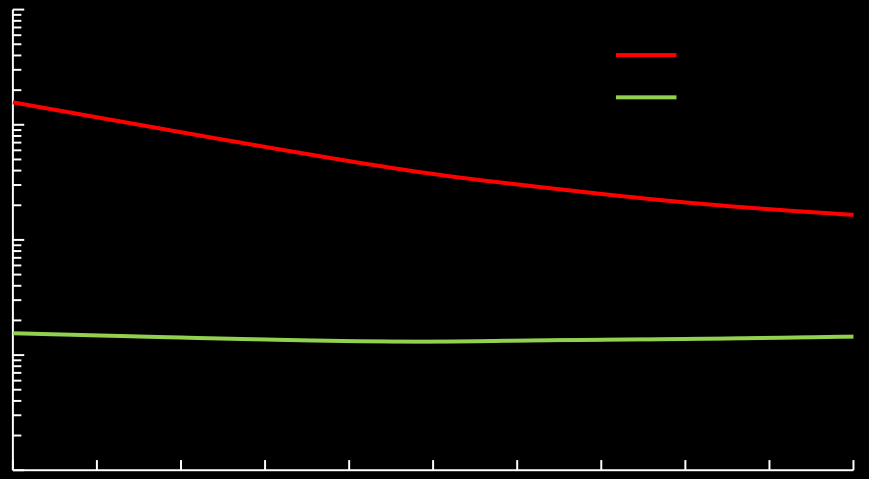
Fmax @ 0.5V	140 MHz
µW/Coremark	2.7

- 3x higher frequency for low latency
- 77% better power efficiency
- Applying Racyics 22FDX® Adaptive Body Bias (ABB) Regulation IP and Methodology

Ultra-low Leakage – across all Temperatures

~1pA/µm in thin-oxide transistors at room temp & reverse body bias keeps leakage ultra-low at high temp

Components of drain leakage current	Temperature dependency
Gate leakage	Weak
Gate induced drain leakage (GIDL)	Moderate
Channel leakage	Strong



Transistor optimization achieves ~1pA/µm leakage at room temperature in 22FDX®

Reverse body bias restores ultra-low leakage at high temperature

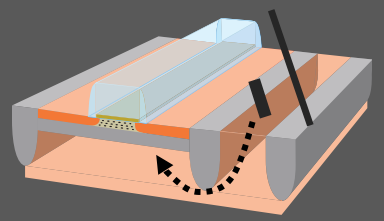
The Industry's Only FD-SOI Body Bias Ecosystem

>30% & growing number of customer product TOs have implemented body bias solutions

Body-bias Enabled

Customer Products

>30%
tape-outs already enabled for body-bias



Design Methodology

GLOBALFOUNDRIES
DOLPHIN INTEGRATION
Racyics

Reference Design Flow

cadence
SYNOPSYS

Foundation IPs

Standard Cells
Memory

Body-bias Generator
Body-bias Controller
PVT Monitors
OTP Memory

SYNOPSYS
invecas
DOLPHIN INTEGRATION
Racyics

Agenda

1

2

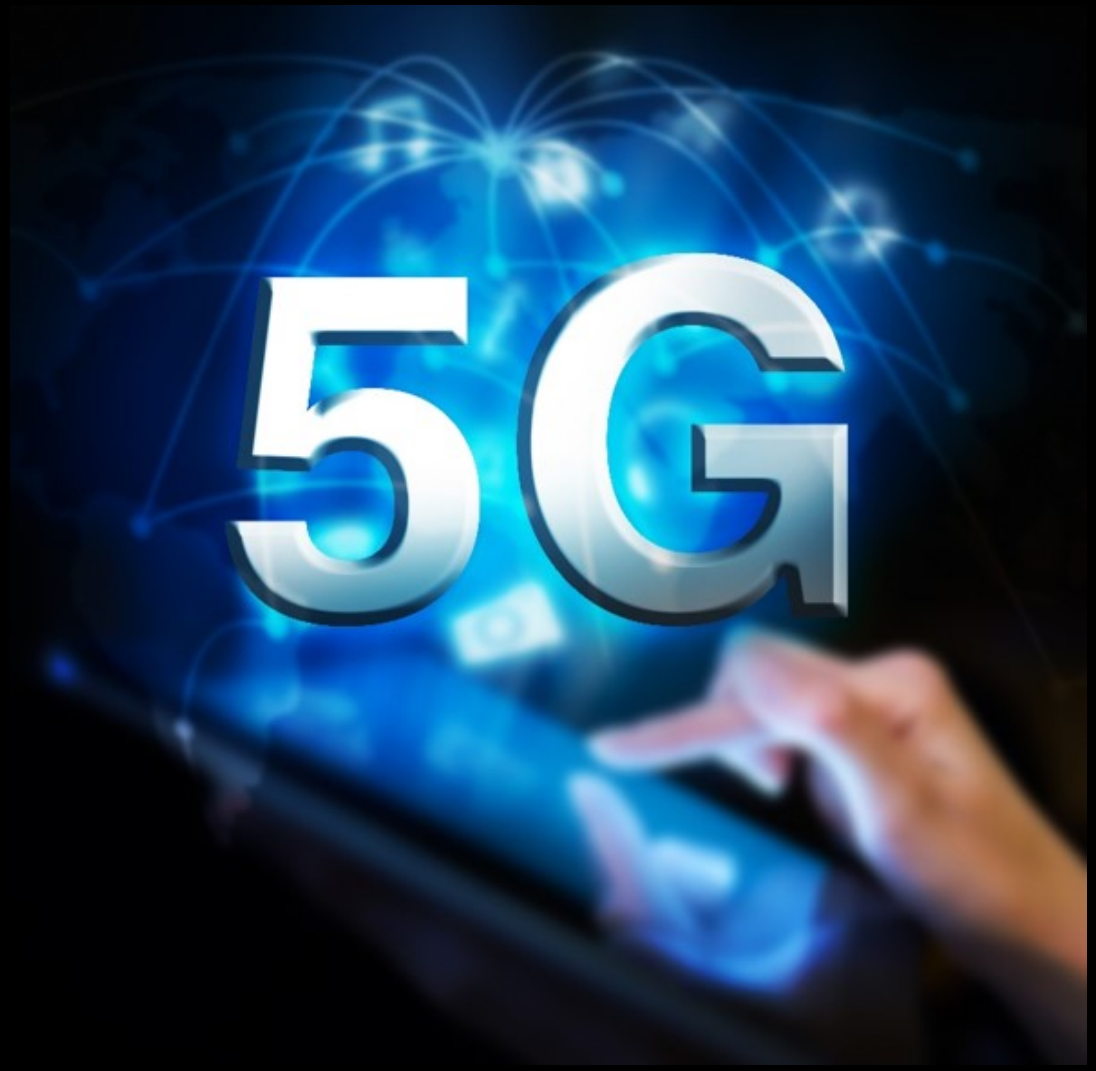
3

4 22FDX: 5G mmWave & Automotive readiness

5

6

Market Application: 5G mmWave



Application: 5G/mmWave mobility and infrastructure

- Platform: 22FDX
- Feature: mmWave

FDX Delivers

- High ft/fmax
- High output power
- Low loss; high power conversion efficiency
- Battery life, signal quality, coverage, low BoM

Total Solution Includes:

- Reference designs for fast TTM
  - mmWave PA via stacked SOI solutions
  - High Pout with high PAE%
  - Low power LNA; low LNA NF and low Switch IL
- Fully enabled and qualified mmWave PDK

22FDX® - the ONLY 5G mmWave solution that enables full integration at the desired performance with system BoM cost savings

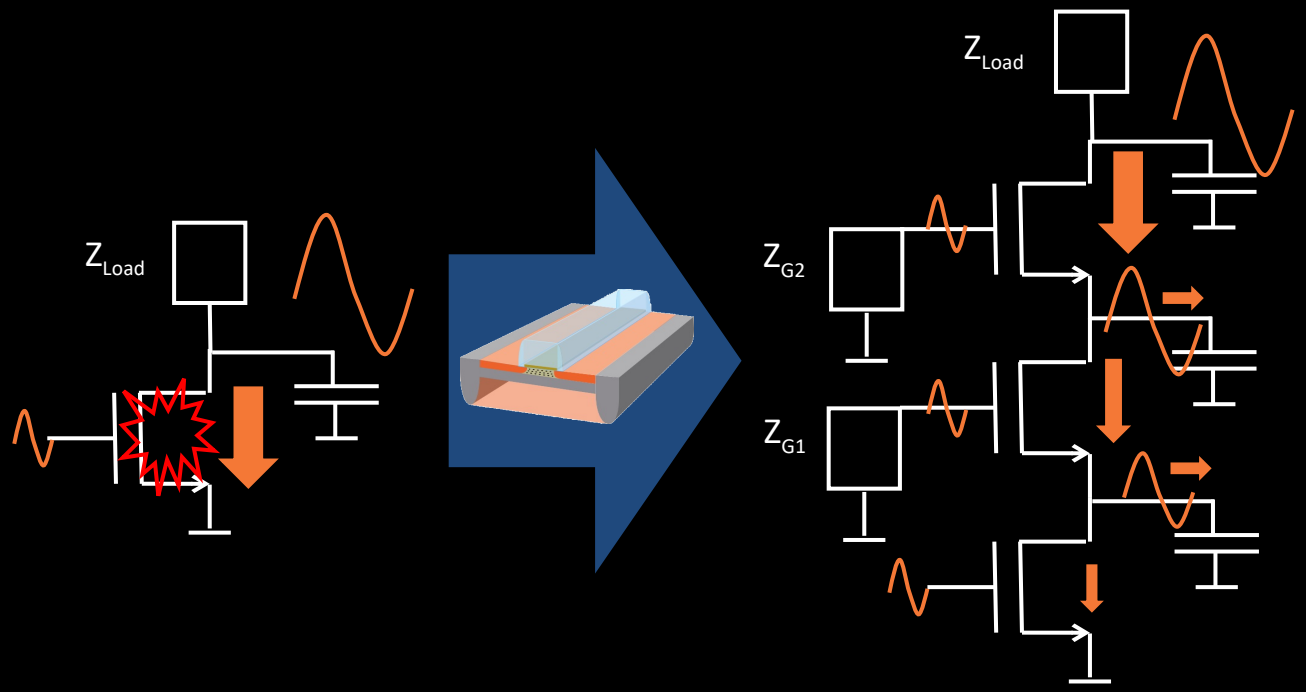
Old bulk CMOS processes fall far short in performance, power, cost and readiness

	GF 22FDX	Old Bulk 28nm CMOS	22FDX ADVANTAGES	Value to GF Clients	Value to Phone OEMs & Carriers
PA	18dBM @ 42% PAE	13dBM @ 34% PAE	**~30% transmit pwr savings ~14% total pwr savings**	▪ Lower power ▪ Better thermal efficiency	▪ 10% better battery life
LNA Noise Figure	1.4dB	>2dB	**≥30% better NF**	▪ Superior signal reach; ▪ ~6% gain in UE distance coverage* ▪ Stronger signal	▪ Less dropped calls ▪ Better call quality ▪ ~6% gain in UE distance coverage*
Switch Insertion Loss	0.65dB	>1.5dB	**≥50% better IL**	▪ Stronger signal	▪ Less dropped calls
Area Scaling	0.8X	1.0X	**20% shrink**	▪ More transistors per die ▪ System BoM cost savings	▪ More features in the same footprint ▪ Device BoM efficiencies

** 28 GHz band, TX and RX antenna gain of 20 dB, line of sight communication*

22FDX® - Unique, High-efficiency Stacking for Power Handling

Enabling best-in-class mmWave power amplifier and switch for integrated 5G SoC



Electrically Isolated Body in FD-SOI Allows Transistor Stacking for Large Signal in PA and Switch

Parameters	Measured	Measured
Stacking	3-Stack PA	2-Stack PA
S21 peak freq (GHz)	27.8	29
IDDQ (mA)	15.9	15.8
Gain (dB)	12.4	12.7
P1dB (dBm)	17.4	15.8
Psat/P3dB (dBm)	18.2	16.4
PAE_Psat-6dB (%)	18.3	20.8
PAE_peak (%)	30.2	41.0
S11	-10.6	-9.9
S22	-2.1	-1.2
Ruggedness Passed	18 dBm	15 dBm

5G 28 GHz Differential PA on 22FDX®

Market application: automotive radar

Best-in-class performance to meet new safety regulations and L4/L5 autonomous driving requirements

Application: automotive RADAR (77GHz)

- Platform: 22FDX
- Feature: mmWave, Auto G1

FDX Delivers

- mmWave performance, low-power, and isolation for improved resolution
- 14dBm Pout w/ only 1dB variation (76-81GHz)
- Edge intelligence for object classification

Total Solution Includes:

- AutoPro™ service package
- Auto grade manufacturing qualification
- AEC-Q100 IP & ISO26262 IP
- Radar reference designs
- Aging aware design (ABB & LVF)

22FDX® - The right technology for next gen ADAS/autonomous radar

Optimal mmWave performance and low-power; more channels for improved resolution, edge processing for object classification

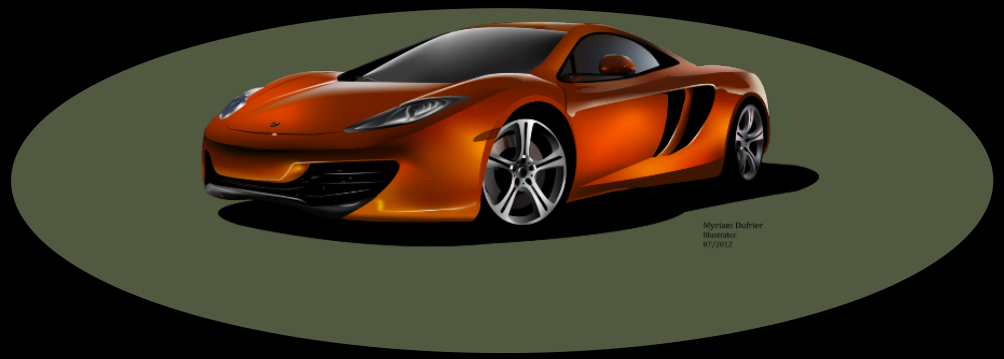
	GF 22FDX	Old Bulk 28nm CMOS	22FDX ADVANTAGES	Value to GF Clients	Value to Auto Tier1 & OEMs
Pout	13dBM @ 15% PAE for PA	12dBM @ up to 10% PAE for PA	**Enabled by efficient stacking 50% higher PAE**	▪ Longer Range vs Bulk ▪ Lower Power @ fixed range	▪ Highest performance Radar ▪ LRR/SRR with single CMOS technology
Pout / Temperature	+/- 1dB	+/- 2dB	**Back Gate Bias for tight Pout control**	▪ Ease to hit performance / temp	▪ Consistent performance in all environments
Transceiver Power	0.6W @ 50% DC 4RX/2TX	1.0W @ 50% DC 4RX/2TX	**40% lower power consumption**	▪ Product spec differentiation ▪ Ease thermal package design	▪ Best Thermal Headroom
Noise Figure	7dB DSB @ 77GHz	16dB DSB @ 77GHz	**9dB better NF**	▪ Lower Power @ fixed range ▪ Longer range @ Pout max	▪ High performance within best thermal budget
Switch Insertion Loss	0.6dB per device @80GHz	1.5dB per device @60GHz	**>25% better sensitivity**	▪ Lower power loss/voltage attenuation ▪ Lower signal degradation ▪ Higher rcvr sensitivity, dyn range	▪ Higher system performance ▪ Higher coverage
Integrated Processing	13dBM @ 15% PAE for PA 1.3x digital perf 0.8x area 0.6x power	12dBM @ up to 10% PAE for PA 1.0x digital perf 1.0x area 1.0x power	**50% higher PAE** **Full node scaling for Digital** **40% lower power**	▪ Smallest sensor size ▪ Max performance at iso power ▪ Reduced system/package cost	▪ Enhanced radar imaging resolution ▪ More features in the same footprint ▪ Device BoM efficiencies

22FDX® auto qualified, ready for production

- Dresden, Fab 1 automotive certified **Q1 2018**
- 22FDX fully qualified for automotive Grade 2
  - AEC Q-100; with ambient temp up to 105°C
- Prototyping ongoing, automotive production tapeouts in 2019
- 22FDX and Arbe Robotics 77GHz high resolution radar chipset
- Features high voltage, eNVM auto grade, RF, mmWave

FDX™ Auto Ecosystem with Leading IP Providers

Enabled for Auto G1/G2; Meets ISO 26262 & AEC Q100



G1 libraries meeting ISO 26262 & AEC Q100

ASIL D ready memory compilers (Via ROM, HD SP SRAM, HD 2PRF, HD 1PRF, UHD 2PRF)

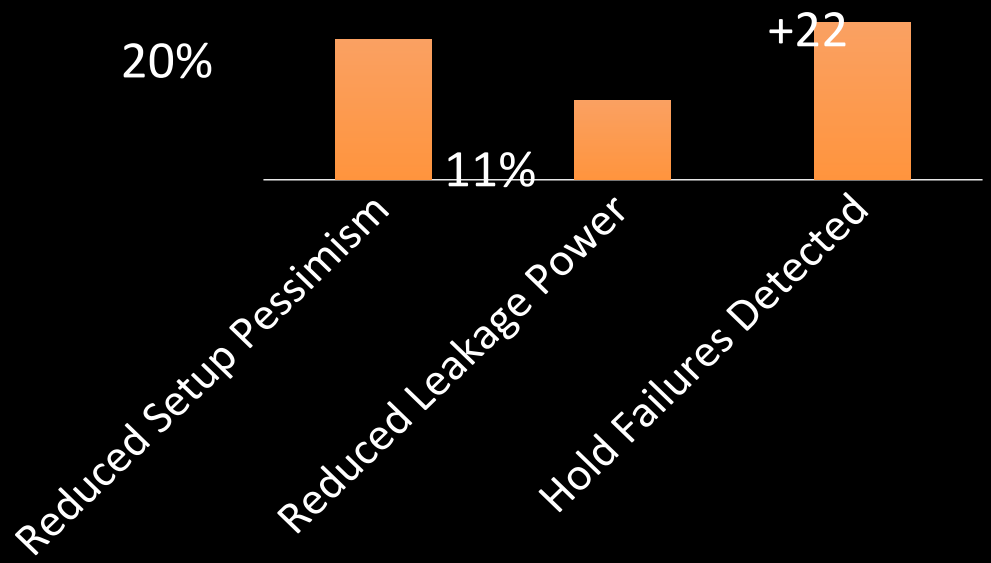
ASIL B ready interface IP (LPDDR4, MIPI, USB 3.1/ PCIe 3.0, USB 2.0, ADC)

AEC-Q100 Ready Grade	Ambient Temp	Junction Temp
1	-40°C to +125°C	-40°C to +150°C
2	-40°C to +105°C	-40°C to +125°C

	Description	SYNOPSYS®	ARAGIO SOLUTIONS	ANALOG BITS	DOLPHIN INTEGRATION
Standard Cells	HP Libraries	●			
	ULP Libraries	●			
Memories	1-Port Register File (1RW)	●			
	2-Port Register File (1R/1W)	●			
	1-Port SRAM (1RW)	●			
	Pseudo-2-Port SRAM (2RW)	●			
	ROM	●			
GPIO	18V33 GPIO		●		
	18V18 GPIO		●		
	18V33 OSC_032		●		
	18V33 OSC		●		
	18V25 LVDS		●		
Interface IP	MIPI D-PHY TX/RX (x4)	●			
	LPDDR4 Combo-PHY	●			
	PCIe 3.1/ USB 3.1 Combo	●			
	USB 2.0 PHY	●			
Analog IP	12-bit ADC	●			
	Wide Range Programmable PLL			●	
	PVTA Sensor			●	●
	Body Bias Generator			●	●

Aging LVF Methodology to Reduce Pessimism in Automotive Designs

- High reliability designs must consider aging effects (HCI, BTI) in design
  - Impacts delay, slew, variability/spread, and Vt
- Adding cell-specific Aging and Variation modeling reduces pessimism and improves accuracy
  - 20% reduction in setup pessimism; enables less conservative design
  - >11% leakage improvement; enabled by more accurate Vt modeling
  - Detects more hold failures, ensures no critical fixes are missed



Aging for Automotive and IoT Applications
2019 Design Automation Conference
Siddharth Sawant, Design Enablement

invecas SYNOPSYS cādence GLOBALFOUNDRIES

Agenda

1

2

3

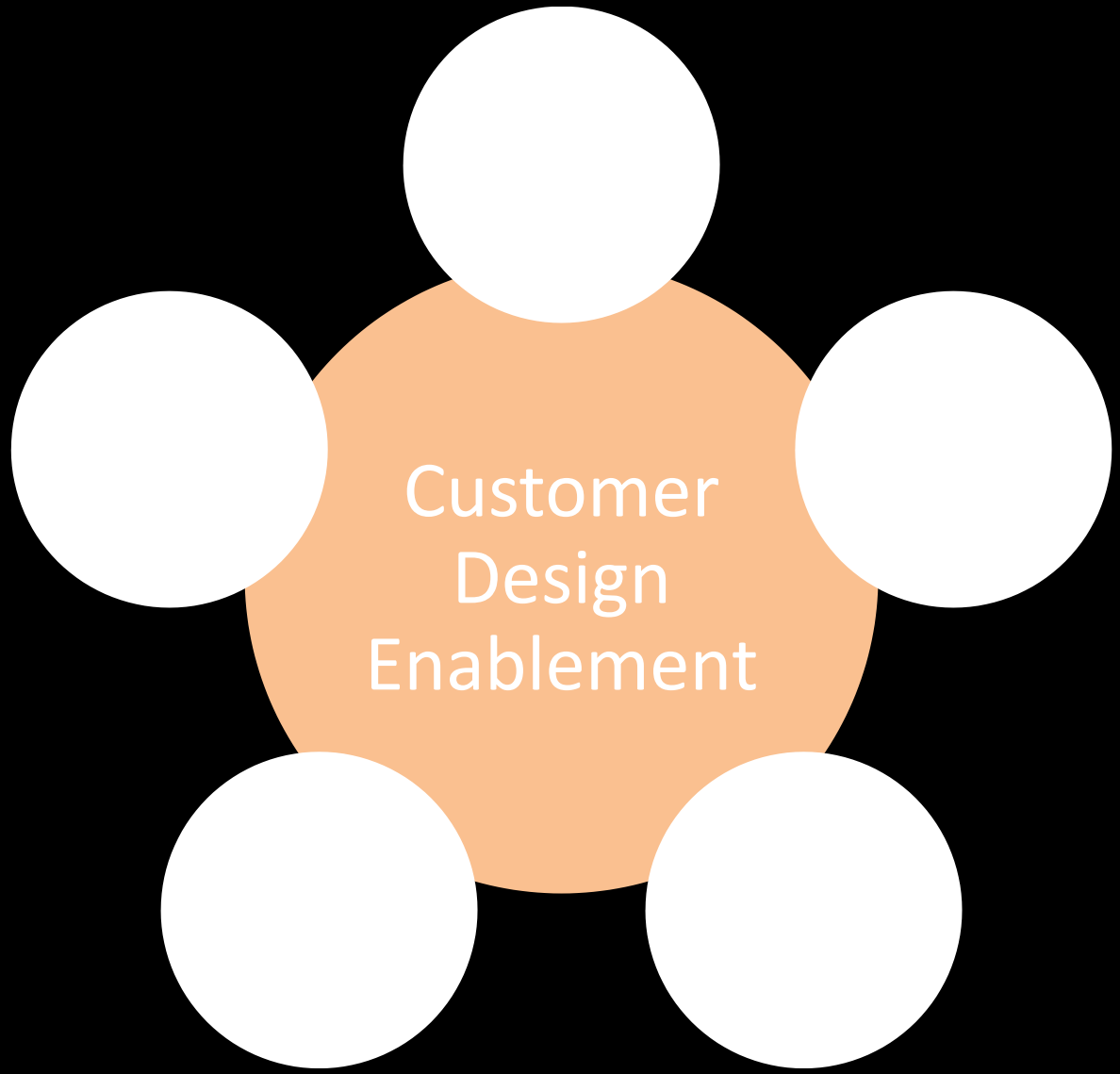
4

5 Customer Design Enablement

6

Customer Design Enablement

- PDK/Spice Model Development, QA & Release
  - CDSLIB, DRC, LVS, PEX, Spice, EMIR, P&R Techfile
- Design Methodology & Reference Flows
- EDA & IP partnerships
- Expert customer support to facilitate easy adoption
- PPA benchmarking for technology entitlement and competitiveness
- Analog/Mixed-Signal & RF Reference designs
- Tapeout operations



CDE Organizational Strategy Streamlined for Customer Success

WorldWide R&D

Technology Enablement

PDKs and Reference flows

Global Sales & Customer Support

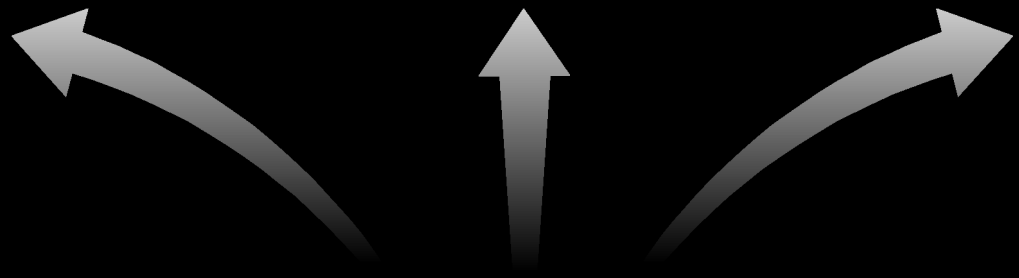
IP Development

Design Services

WorldWide Operations

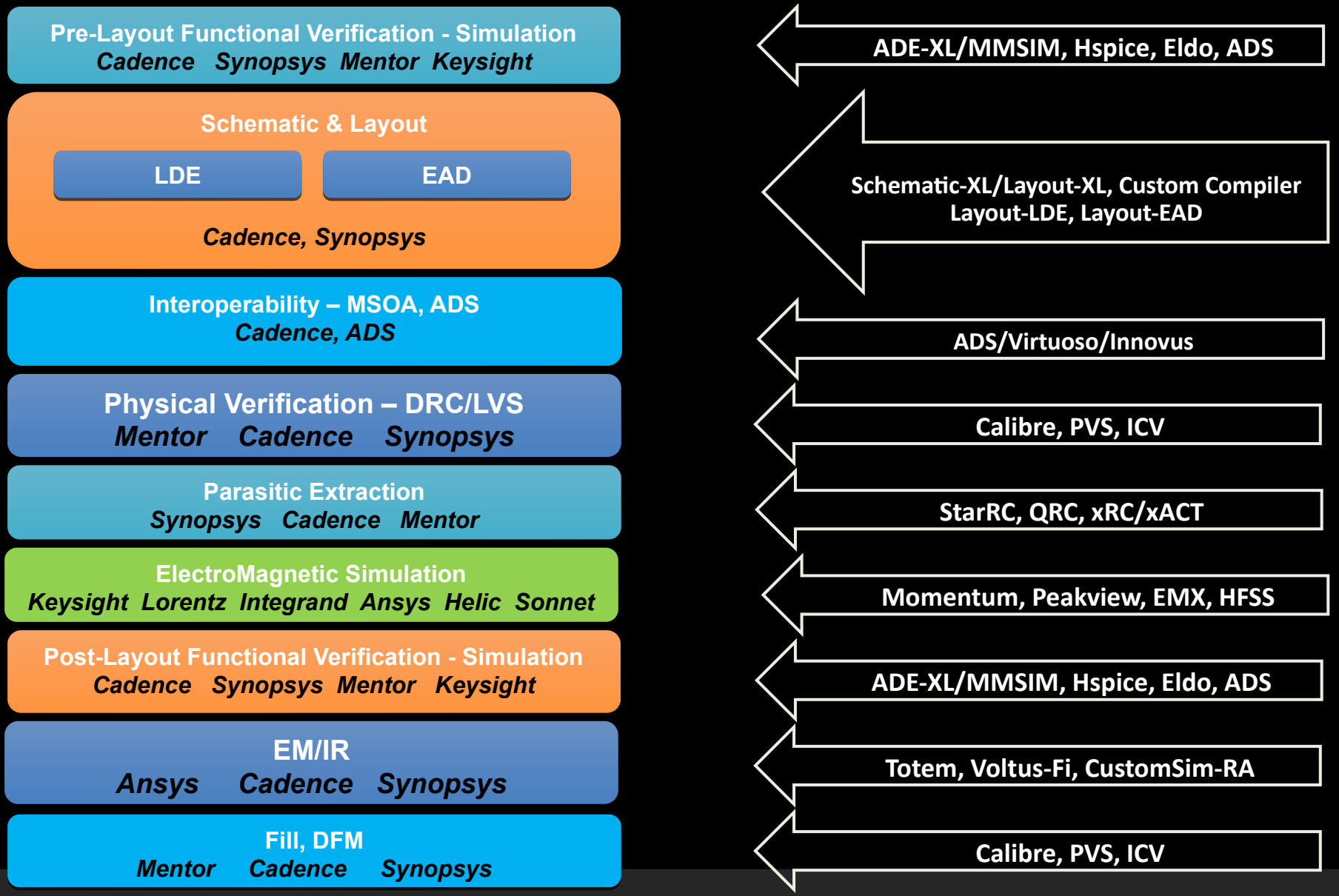
Tapeout Operations

Photomask Operations



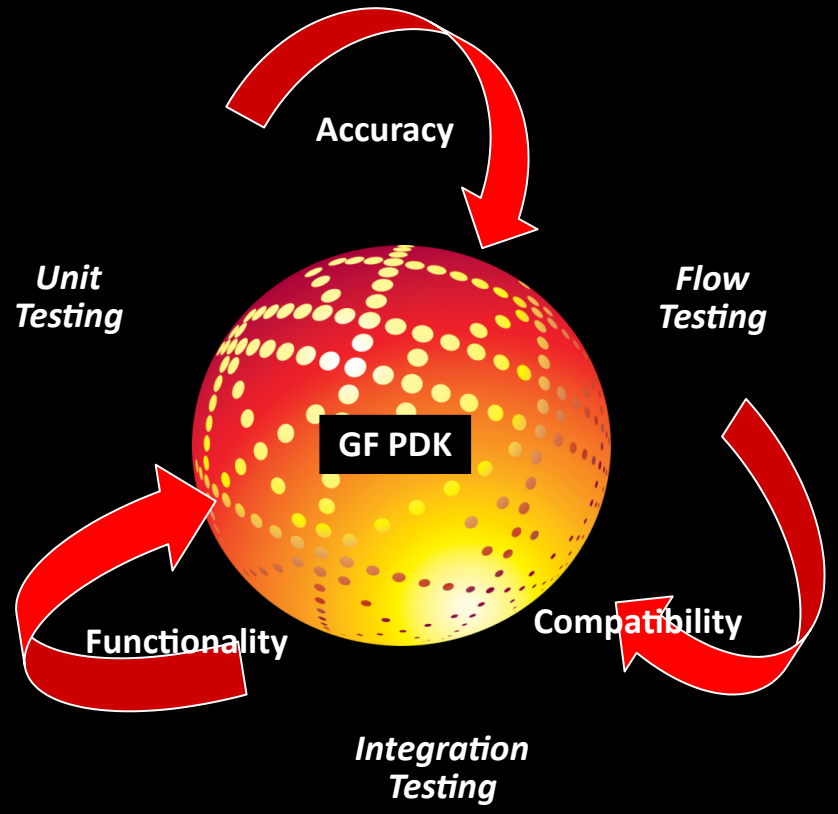
Customer Design Enablement

Typical Custom Design Flow



PDKs with focus on Quality

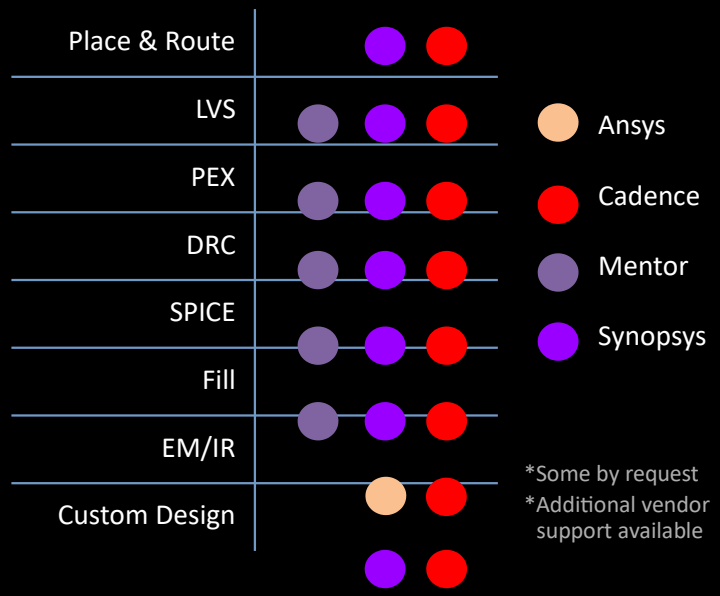
- GLOBALFOUNDRIES PDKs have wide coverage of industry standard tools & flows
  - Enables designers to choose appropriate tool flow per requirement
- Significant Quality Assurance steps to ensure
  - Accuracy
  - Functionality
  - Flow compatibility
  - Ease of use
  - Consistency
- Need for automated tools to handle volume of tests combined with permutations of tools and flows to be validated
  - Increased complexity at advanced nodes – 22FDX, 12LP



Reference Flows Enablement

Synopsys Certified Reference Flow

SYNTHESIS	Design Compiler
FORMAL VERIFICATION	Formality (RTL vs Gate Netlist)
PLACE & ROUTE	IC Compiler, IC Compiler II IC Validator (In-design)
FORMAL VERIFICATION	Formality (Gate \vs Routed Netlist)
PEX	StarRC
STA	PrimeTime



Std cell lib PDK

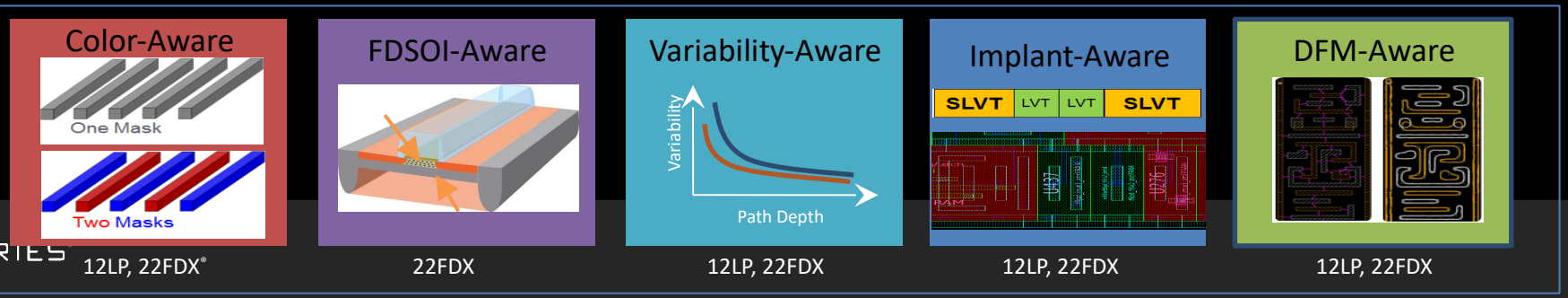
Cadence Certified Reference Flow

SYNTHESIS	Genus
FORMAL VERIFICATION	Conformal (RTL vs Gate Netlist)
PLACE & ROUTE	Innovus PVS (In-design)
FORMAL VERIFICATION	Conformal (Gate vs Routed Netlist)
PEX	Quantus
STA EMIR	Tempus Voltus

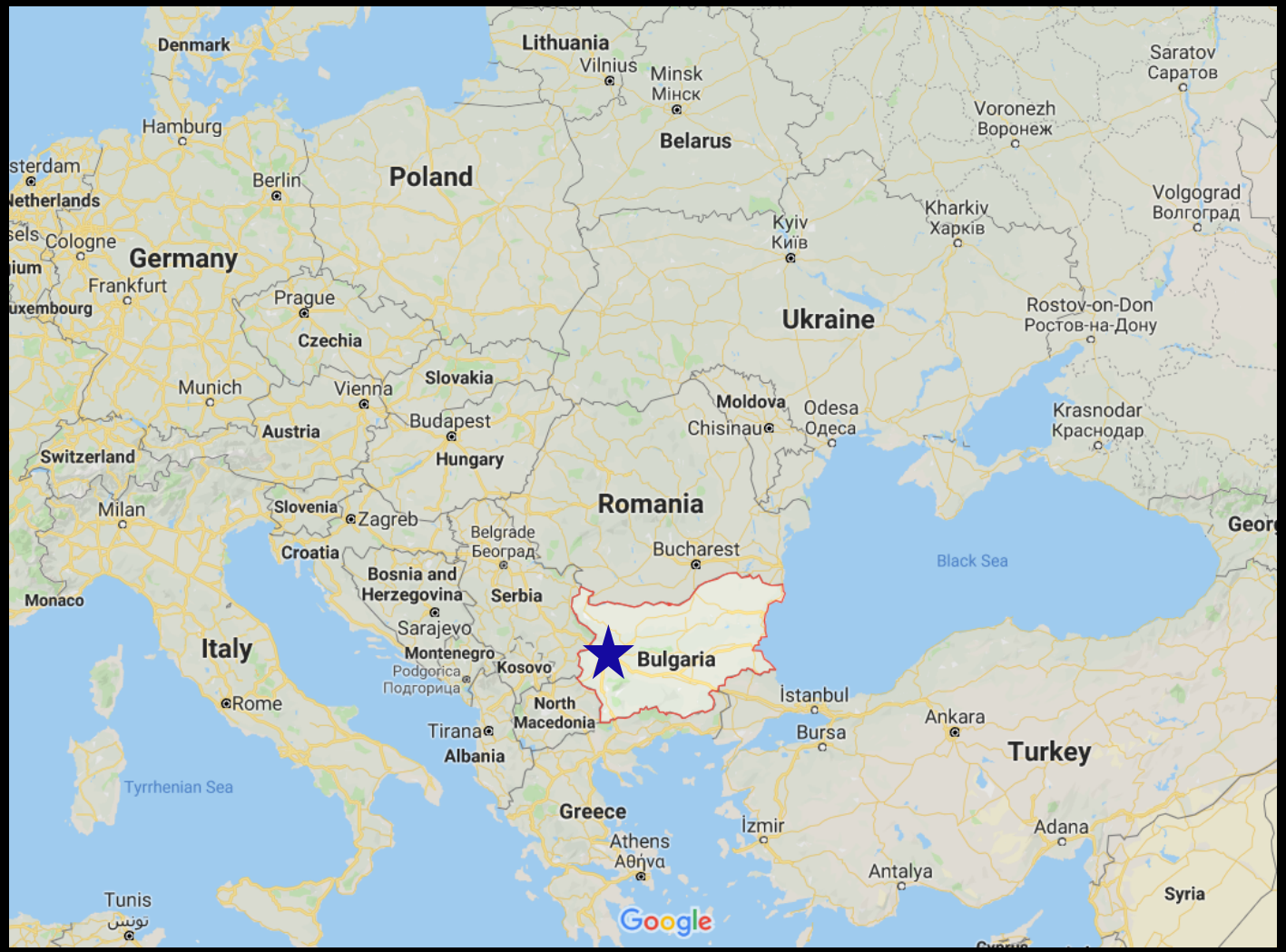
Tape-out proven Flow

GF Digital Design Reference Flow

Includes sample block tested at all RTL-to-GDS steps with Sign-off

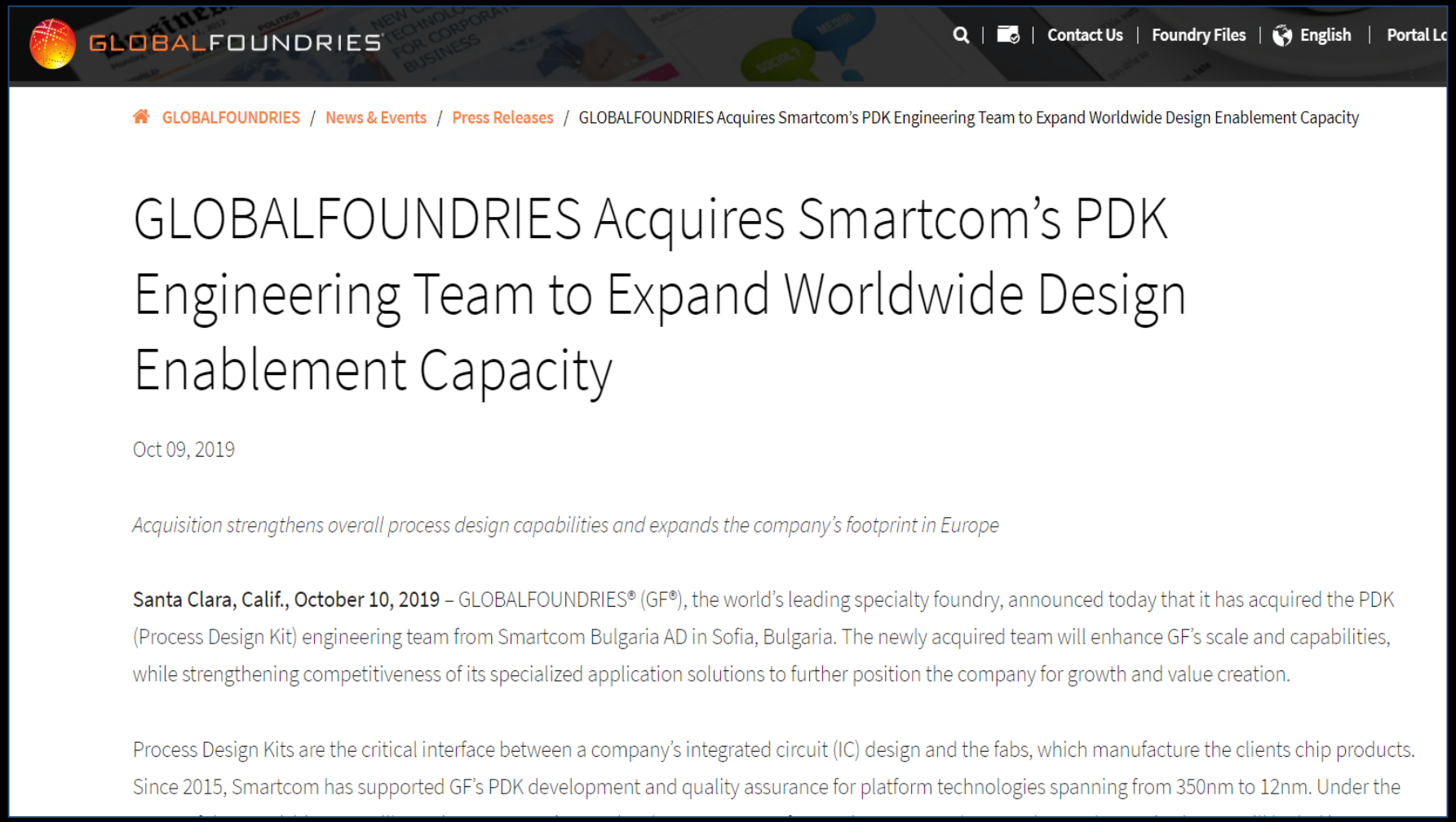


GLOBALFOUNDRIES CDE in Bulgaria



- Over 100 strong engineering team in Sofia
- Primary focus on Customer Design Enablement – PDK development & QA
- Deep technical expertise in EDA tools
  - Cadence, Mentor, Synopsys, Ansys & others
- Tight collaboration with Academia
- Strong Co-op program to transition graduating students to the real world with focused training and work assignments

Fortifying PDK Workforce via Smartcom Acquisition



GLOBALFOUNDRIES

Contact Us | Foundry Files | English | Portal Lo

GLOBALFOUNDRIES / News & Events / Press Releases / GLOBALFOUNDRIES Acquires Smartcom's PDK Engineering Team to Expand Worldwide Design Enablement Capacity

GLOBALFOUNDRIES Acquires Smartcom's PDK Engineering Team to Expand Worldwide Design Enablement Capacity

Oct 09, 2019

Acquisition strengthens overall process design capabilities and expands the company's footprint in Europe

Santa Clara, Calif., October 10, 2019 – GLOBALFOUNDRIES® (GF®), the world's leading specialty foundry, announced today that it has acquired the PDK (Process Design Kit) engineering team from Smartcom Bulgaria AD in Sofia, Bulgaria. The newly acquired team will enhance GF's scale and capabilities, while strengthening competitiveness of its specialized application solutions to further position the company for growth and value creation.

Process Design Kits are the critical interface between a company's integrated circuit (IC) design and the fabs, which manufacture the clients chip products. Since 2015, Smartcom has supported GF's PDK development and quality assurance for platform technologies spanning from 350nm to 12nm. Under the

Agenda

1

2

3

4

5

6 Summary

2009
GF Created

2010
- Acquires Chartered Semiconductor

2011

2012
- Fab 8 delivers initial silicon first time right
- Dresden ships 250,000th 32 nm HKMG wafer

2013
- Launches 14 nm FinFET technology

2014
- Collaborates with Samsung on 14 nm manufacturing

2015
- Acquires IBM Microelectronics business
- Launches: 22FDX® FD-SOI platform, FX-14™ ASIC

2016
- Announces 12FDX™
- Launches: SiGe 8XP and 5PAx, 22FDX®-MRAM technology, FDXcelerator™ partner program

2017
- Announces AutoPro™ service package
- Launches 12 nm FinFET (12LP), 8SW and 45RFSOI

2018
- Announces differentiated foundry strategy
- Announces SiPh roadmap
- Launches RFwave™ ecosystem
- Establishes ASIC subsidiary

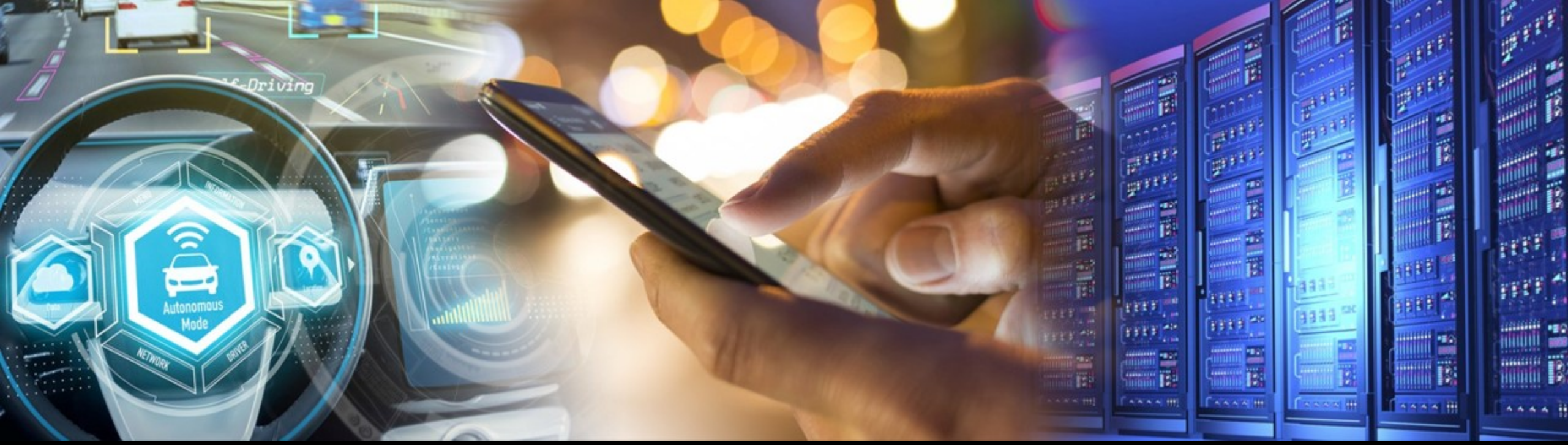
2019
10 Year Corporate Anniversary

Summary

- GLOBALFOUNDRIES is setting new trends of innovation in the semiconductor industry through differentiation
- 22FDX® - the *only planar* technology in production that has enabled CMOS scaling below 28nm
  - Delivers FinFET-like performance/power efficiency, 0.4V ULP, and 1pA/um ULL
  - Enables mmWave LNA with record-low power, best-in-class 5G mmWave PA
  - Single, unified technology platform – best suited for architectural innovations in Automotive and 5G mmWave designs
- Streamlined Customer Design Enablement organization for Client success
- PDK, Models and Design Flows form the fundamental core of Customer Design Enablement

Changing *the industry*
that's ***Changing*** *the world*

GLOBALFOUNDRIES®



Thank you

GLOBALFOUNDRIES®